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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,204	09/15/2003	H. Bernhard Pogge	FIS920020007	2203
32074	7590	07/01/2004	EXAMINER	
INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			CHAMBLISS, ALONZO	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/605,204

Applicant(s)

POGGE ET AL.

Examiner

Alonzo Chambliss

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 08 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 21-26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2 and 3.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election of claims 1-20 in the reply filed on 4/8/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 21-26 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim.

### ***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on 9/15/03 and 10/16/03 was filed before the mailing date of the non-final rejection on 6/28/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Drawings***

3. The formal drawings filed on 9/15/03 have been approved by the examiner.

### ***Specification***

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is

suggested: " METHOD OF FABRICATING INTEGRATED ELECTRONIC CHIP WITH  
AN INTERCONNECT DEVICE ".

### ***Claim Objections***

5. Claim 1 is objected to because of the following informalities: in line 15 the word  
"the other " should be changed to -- one --. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that  
form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public  
use or on sale in this country, more than one year prior to the date of application for patent in the United  
States.

7. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by  
Pogge et al. (IBM Microelectronics).

With respect to Claims 1 and 12, Pogge teaches forming a first layer on a plate  
transparent to ablating radiation, the first layer having a first set of conductors disposed  
therein, the first set of conductors connecting to bonding pads, the bonding pads being  
spaced with a first spacing distance in accordance with a required spacing of  
connections to the motherboard', forming a second layer on the semiconductor device,  
the second layer having a second set of conductors disposed therein connecting to the  
semiconductor device, first layer and the second forming studs on one of the layer and  
a third layer on one of the first layer and the second layer, the studs being spaced with

a second spacing distance less than the first spacing distance', forming vias in the third layer, the vias being spaced in accordance with the second spacing distance, aligning the studs to the vias; attaching the semiconductor that the first set of conductors and the second set of device to the first layer, so conductors are connected through the studs', ablating an interface between the first layer and the plate using ablating radiation transmitted through the plate, thereby detaching the plate; and attaching the connector structures to the bonding pads (see entire disclosure and figures).

With respect to Claims 2 and 13, Pogge teaches attaching a support structure to the first layer, so that the support structure surrounds the semiconductor device (see entire disclosure and figures).

With respect to Claims 3 and 14, Pogge teaches wherein the connector structures form one of a pin grid array (PGA), a ball grid array (BGA), a C4 array and a land grid array (LGA) (see entire disclosure and figures).

With respect to Claims 4 and 15, Pogge teaches wherein the step of attaching the support structure is performed before the step of attaching the semiconductor device and before the ablating step (see entire disclosure and figures).

With respect to Claim 5, Pogge teaches wherein the step of attaching the support structure is performed after the step of attaching the semiconductor device and before the ablating step (see entire disclosure and figures).

With respect to Claims 6 and 16, Pogge teaches wherein the mother board is characterized by a thermal coefficient of expansion (TCE), and the support structure is

provided with a TCE approximately that of the motherboard (see entire disclosure and figures).

With respect to Claims 7 and 17, Pogge teaches wherein the support structure has an area corresponding to an area occupied by the bonding pads (see entire disclosure and figures).

With respect to Claims 8, Pogge teaches further comprising the step of filling a gap between the semiconductor device and the surrounding support structure (see entire disclosure and figures).

With respect to Claims 9 and 19, Pogge teaches further step of exposing the comprising the bonding pads, before said step of attaching the connector structures (see entire disclosure and figures).

With respect to Claim 10, Pogge teaches wherein the studs are formed on the first layer, and the first layer is provided with an adhesive layer for bonding to the third layer (see entire disclosure and figures).

With respect to Claims 11 and 20, Pogge teaches wherein the second set of conductors is arranged in a plurality of metal layers, the number of the metal layers being less than a number of layers required for fan out to the bonding pads spaced with the first spacing distance (see entire disclosure and figures).

With respect to Claim 18, Pogge teaches further comprising the step of filling a gap between the semiconductor device and the support structure and a gap between the semi-conductor device and the first layer surrounding the C4 connectors (see entire disclosure and figures).

### ***Double Patenting***

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-20 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,444,560.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application and the patent recite a plate transparent to ablating radiation with studs aligned in a via.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

### ***Conclusion***

10. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.



Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

**AC**/June 28, 2004



Alonzo Chambliss  
Primary Patent Examiner  
Art Unit 2827